8 – BIT LOAD GROUP

Mnemonic	Symbolic Operation	Flags								Op-Code				No. of Bytes	No. of M Cycles	No. of T States	Comments	
		S	Z		H		P/V	N	C	76	543	210	Hex					
LD r, s	r←s	•	•	X	•	X	•	•	•	01	r	s		1	1	4	r, s	Reg.
LD r, n	r←n	•	•	X	•	X	•	•	•	00	r	110		2	2	7	000	B
										←	n	→					001	C
LD r, (HL)	r←(HL)	•	•	X	•	X	•	•	•	01	r	110		1	2	7	010	D
LD r, (IX + d)	r←(IX + d)	•	•	X	•	X	•	•	•	11	011	101	DD	3	5	19	011	E
										01	r	110					100	H
										←	d	→					101	L
LD r, (IY + d)	r←(IY + d)	•	•	X	•	X	•	•	•	11	111	101	FD	3	5	19	111	A
										01	r	110						
										←	d	→						
LD (HL), r	(HL)←r	•	•	X	•	X	•	•	•	01	110	r		1	2	7		
LD (IX + d), r	(IX + d) ←r	•	•	X	•	X	•	•	•	11	011	101	DD	3	5	19		
										01	110	r						
										←	d	→						
LD (IY + d), r	(IY + d) ←r	•	•	X	•	X	•	•	•	11	111	101	FD	3	5	19		
										01	110	r						
										←	d	→						
LD (HL), n	(HL) ←n	•	•	X	•	X	•	•	•	00	110	110	36	2	3	10		
										←	n	→						
LD (IX + d), n	(IX + d) ←n	•	•	X	•	X	•	•	•	11	011	101	DD	4	5	19		
										00	110	110	36					
										←	d	→						
										←	n	→						
LD (IY + d), n	(IY + d) ←n	•	•	X	•	X	•	•	•	11	111	101	FD	4	5	19		
										00	110	110	36					
										←	d	→						
										←	n	→						
LD A, (BC)	A ←(BC)	•	•	X	•	X	•	•	•	00	001	010	0A	1	2	7		
LD A, (DE)	A ←(DE)	•	•	X	•	X	•	•	•	00	011	010	1A	1	2	7		
LD A, (nn)	A ←(nn)	•	•	X	•	X	•	•	•	00	111	010	3A	3	4	13		
										←	n	→						
										←	n	→						
LD (BC), A	(BC) ←A	•	•	X	•	X	•	•	•	00	000	010	02	1	2	7		
LD (DE), A	(DE) ←A	•	•	X	•	X	•	•	•	00	010	010	12	1	2	7		
LD (nn), A	(nn) ←A	•	•	X	•	X	•	•	•	00	110	010	32	3	4	13		
										←	n	→						
										←	n	→						
LD A, I	A ←I	↕	↕	X	0	X	IFF	0	•	11	101	101	ED	2	2	9		
										01	010	111	57					
LD A, R	A ←R	↕	↕	X	0	X	IFF	0	•	11	101	101	ED	2	2	9		
										01	011	111	5F					
LD I, A	I ←A	•	•	X	•	X	•	•	•	11	101	101	ED	2	2	9		
										01	000	111	47					
LD R, A	R ←A	•	•	X	•	X	•	•	•	11	101	101	ED	2	2	9		
										01	001	111	4F					

Note: r, s means any of the registers A, B, C, D, E, H, L

IFF the content of the interrupt enable filip-flop (IFF) is copid into the P/V Flag

Flag Notation: • = flag not affected, 0 = flag is reset, 1 = flag is set,

↕ = flag is affcted according to the result of the operation

16 – BIT LOAD GROUP

Mnemonic	Symbolic Operation	Flags								Op-Code				No. of Bytes	No. of M Cycles	No. of T States	Comments
		S	Z		H		P/V	N	C	76	543	210	Hex				
LD dd, nn	dd ← nn	•	•	X	•	X	•	•	•	00	dd0	001		3	3	10	dd Pair
										←	n	→					00 BC
										←	n	→					01 DE
LD IX, nn	IX ←nn	•	•	X	•	X	•	•	•	11	011	101	DD	4	4	14	10 HL
										00	100	001	21				11 SP
										←	n	→					
										←	n	→					
LD IY, nn	IY←nn	•	•	X	•	X	•	•	•	11	111	101	FD	4	4	14	
										00	100	001	21				
										←	n	→					
										←	n	→					
LD HL, (nn)	$H \leftarrow (nn + 1)$	•	•	X	•	X	•	•	•	00	101	010	2A	3	5	16	
	$L \leftarrow (nn)$									←	n	→					
										←	n	→					
LD dd, (nn)	$dd_H \leftarrow (nn +1)$	•	•	X	•	X	•	•	•	11	101	101	ED	4	6	20	
	$dd_L \leftarrow (nn)$									01	dd1	011					
										←	n	→					
										←	n	→					
LD IX, (nn)	$IX_H \leftarrow nn +1)$	•	•	X	•	X	•	•	•	11	011	101	DD	4	6	20	
	$IX_L \leftarrow (nn)$									00	101	010	2A				
										←	n	→					
										←	n	→					
LD IY, (nn)	$IY_H \leftarrow (nn +1)$	•	•	X	•	X	•	•	•	11	111	101	FD	4	6	20	
	$IY_L \leftarrow (nn)$									00	101	010	2A				
										←	n	→					
										←	n	→					
LD (nn), HL	$(nn + 1) \leftarrow H$	•	•	X	•	X	•	•	•	00	100	010	22	3	5	16	
	$(nn) \leftarrow L$									←	n	→					
										←	n	→					
LD (nn), dd	$(nn+1) \leftarrow dd_H$	•	•	X	•	X	•	•	•	11	101	101	ED	4	6	20	
	$(nn) \leftarrow dd_L$									01	dd0	011					
										←	n	→					
										←	n	→					
LD (nn), IX	$(nn+1) \leftarrow IX_H$	•	•	X	•	X	•	•	•	11	011	101	DD	4	6	20	
	$(nn) \leftarrow IX_L$									00	110	010	22				
										←	n	→					
										←	n	→					
LD (nn), IY	$(nn+1) \leftarrow IY_H$	•	•	X	•	X	•	•	•	11	111	101	FD	4	6	20	
	$(nn) \leftarrow IY_L$									00	100	010	22				
										←	n	→					
										←	n	→					
LD SP, HL	SP ← HL	•	•	X	•	X	•	•	•	11	111	001	F9	1	1	6	
LD SP, IX	SP ← IX	•	•	X	•	X	•	•	•	11	011	101	DD	2	2	10	
										11	111	001	F9				
LD SP, IY	SP ← IY	•	•	X	•	X	•	•	•	11	111	101	FD	2	2	10	
										11	111	001	F9				qq Pair
PUSH qq	$(SP.2) \leftarrow qq_L$	•	•	X	•	X	•	•	•	11	qq0	101		1	3	11	00 BC
	$(SP.1) \leftarrow qq_H$																01 DE
PUSH IX	$(SP.2) \leftarrow IX_L$	•	•	X	•	X	•	•	•	11	011	101	DD	2	4	15	10 HL
	$(SP.1) \leftarrow IX_H$									11	100	101	E5				11 AF
PUSH IY	$(SP.2) \leftarrow IY_L$	•	•	X	•	X	•	•	•	11	111	101	FD	2	4	15	
	$(SP.2) \leftarrow IY_H$									11	100	101	E5				
POP qq	$qq_H \leftarrow (SP+1)$	•	•	X	•	X	•	•	•	11	qq0	001		1	3	10	
	$qq_L \leftarrow (SP)$																
POP IX	$IX_H \leftarrow (SP+1)$	•	•	X	•	X	•	•	•	11	011	101	DD	2	4	14	
	$IX_L \leftarrow (SP)$									11	100	001	E1				
POP IY	$IY_H \leftarrow (SP+1)$	•	•	X	•	X	•	•	•	11	111	101	FD	2	4	14	
	$IY_L \leftarrow (SP)$									11	100	001	E1				

Note: dd is any of the register pairs BC, DE, HL, SP
qq is any of the register pairs AF, BC, DE, HL
$(PAIR)_H$.$(PAIR)_L$ refer to high order and low order eight bits of the register pair respectively
e.g. $BC_L = C$. $AF_H = A$

Flog Notation • flag not affected, 0 = flag reset, 1 = flag set, X = flag is unknown.
flag is affected according to the result of the operation.

EXCHANGE GROUP AND BLOCK TRANSFER AND SEARCH GROUP

Mnemonic	Symbolic Operation	Flags S	Z		H		P/V	N	C	Op-Code 76	543	210	Hex	No. of Bytes	No. of M Cycles	No. of T States	Comments
EX DE, HL	DE↔HL	•	•	X	•	X	•	•	•	11	101	011	EB	1	1	4	
EX AF, AF'	AF ↔AF'	•	•	X	•	X	•	•	•	00	001	000	08	1	1	4	
EXX	BC↔BC' DE↔DE' HL↔HL'	•	•	X	•	X	•	•	•	11	011	001	D9	1	1	4	Register bank and auxiliary register bank exchange
EX (SP), HL	H ↔ (SP+1) L ↔ (SP)	•	•	X	•	X	•	•	•	11	100	011	E3	1	5	19	
EX (SP), IX	IX_H ↔ (SP+1) IX_L ↔ (SP)	•	•	X	•	X	•	•	•	11 11	011 100	101 011	DD E3	2	6	23	
EX (SP), IY	IY_H ↔ (SP+1) IY_L ↔ (SP)	•	•	X	•	X	•	•	•	11 11	111 100	101 011	FD E3	2	6	23	
LDI	(DE) ←(HL) DE ← DE+1 HL ← HL+1 BC ← BC-1	•	•	X	0	X	① ↕	0	•	11 10	101 100	101 000	ED AD	2	4	16	Load (HL) intro (DE), increment the pointers and decrment the byte counter (BC)
LDIR	(DE) ←(HL) DE ← DE+1 HL ← HL+1 BC ← BC-1 Repeat until BC = 0	•	•	X	0	X	0	0	•	11 10	101 110	101 000	ED B0	2 2	5 4	21 16	if BC ≠ 0 if BC = 0
LDD	(DE) ←(HL) DE ← DE-1 HL ← HL-1 BC ← BC-1	•	•	X	0	X	① ↕	0	•	11 10	101 101	101 000	ED A8	2	4	16	
LDDR	(DE) ←(HL) DE ← DE-1 HL ← HL-1 BC ← BC-1 Repeat until BC = 0	•	•	X	0	X	0	0	•	11 10	101 111	101 000	ED B8	2 2	5 4	21 16	if BC ≠ 0 if BC = 0
CPI	A ← (HL) HL ← HL+1 BC ← BC-1	↕	② ↕	X	↕	X	① ↕	1	•	11 10	101 100	101 001	ED A1	2	4	16	
CPIR	A ← (HL) HL ← HL+1 BC ← BC-1 Repeat until A = (HL) or BC = 0	↕	② ↕	X	↕	X	① ↕	1	•	11 10	101 110	101 001	ED B1	2 2	5 4	21 16	if BC ≠ 0 and A ≠(HL) if BC = 0 or A =(HL)
CPD	A ← (HL) HL ← HL-1 BC ← BC-1	↕	② ↕	X	↕	X	① ↕	1	•	11 10	101 101	101 001	ED A9	2	4	16	
CPDR	A ← (HL) HL ← HL-1 BC ← BC-1 Repeat until A = (HL) or BC = 0	↕	② ↕	X	↕	X	① ↕	1	•	11 10	101 111	101 001	ED B9	2 2	5 4	21 16	if BC ≠ 0 and A ≠(HL) if BC = 0 or A =(HL)

Note: ① /V flag is 0 if th result of BC-1 = 0, otherwise P/V = 1
② flag is 1 if A = (HL), otherwis Z = 0.

Flog Notation • = flag not affected, 0 = flag reset, 1 = flag set, X = flag is unknown.
↕ = flag is affected according to the result of the operation.

8 - BIT ARITHMETIC AND LOGICAL GROUP

Mnemonic	Symbolic Operation	Flags								Op-Code				No. of Bytes	No. of M Cycles	No. of T States	Comments
		S	Z		H		P/V	N	C	76	543	210	Hex				
ADD A, r	A ← A + r	↕	↕	X	↕	X	V	0	↕	10	000	r		1	1	4	r Reg.
ADD A, n	A ← A + n	↕	↕	X	↕	X	V	0	↕	11	000	110		2	2	7	000
										←	n	→					001
																	010
ADD A, (HL)	A ← A + (HL)	↕	↕	X	↕	X	V	0	↕	10	000	110		1	2	7	011
ADD A, (IX+d)	A ←A+(IX+d)	↕	↕	X	↕	X	V	0	↕	11	011	101	DD	3	5	19	100 H
										10	000	110					101 L
										←	d	→					111 A
ADD A, (IY+d)	A ←A+(IY+d)	↕	↕	X	↕	X	V	0	↕	11	111	101	FD	3	5	19	
										10	000	110					
										←	d	→					
ADC A, s	A← A+ s + CY	↕	↕	X	↕	X	V	0	↕		001						s is any of r, n, (HL
SUB s	A← A - s	↕	↕	X	↕	X	V	1	↕		010						(IX+d), (IY+d), p, q,
SBC A, s	A← A - s - CY	↕	↕	X	↕	X	V	1	↕		011						as shown for the
AND s	A← A AND s	↕	↕	X	1	X	P	0	0		100						ADD instruction.
OR s	A← A OR s	↕	↕	X	↕	X	P	0	0		110						The indicatedbits
XOR s	A← A XOR s	↕	↕	X	↕	X	P	0	0		101						replace the 000
CP s	A← s	↕	↕	X	↕	X	V	1	↕		111						the ADD set above
INC r	r ←r + 1	↕	↕	X	↕	X	V	0	•	00	r	100		1	1	4	
INC (HL)	(HL) ←(HL)+1	↕	↕	X	↕	X	V	0	•	00	110	100		1	3	11	
INC (IX+d)	(IX+d) ←	↕	↕	X	↕	X	V	0	•	11	011	101	DD	3	6	23	
	(IX+d) + 1									00	110	100					
										←	d	→					
INC (IY+d)	(IY+d) ←	↕	↕	X	↕	X	V	0	•	11	111	101	FD	3	6	23	
	(IY+d) + 1									00	110	100					
										←	d	→					s is any of r, (HL),
DEC s	s ←s - 1	↕	↕	X	↕	X	V	1	•			101					(IX+d) , (IY+d) as
																	shown for INC.
																	DEC same format
																	and states as INC.
																	Repkace 1π0 ØìtH
																	101 ìn Op-CodŜ

Note: The V symbol in the P/V flag column indicates that the P/V flag contains the overflow of the result of the operation. Smilarly the P symbol indicates parity. V = 1 means overflow, V = 0 means not overflow, P = 1 means parity of the resuly is evn. P = 0 means parity of the result is odd.

Flog Notation • = flag not affected, 0 = flag reset, 1 = flag set, X = flag is unknown.
↕ = flag is affected according to the result of the operation.

Mnemonic	Symbolic Operation	Flags								Op-Code				No. of Bytes	No. of M Cycles	No. of T States	Comments
		S	Z		H		P/V	N	C	76	543	210	Hex				
DAA	Converts acc. content into packed BCD following add or subtract with packed BCD operands.	↕	↕	X	↕	X	P	•	↕	00	100	111	27	1	1	4	Decimal adjust accumulator
CPL	A← $\overline{A}$	•	•	X	1	X	•	1	•	00	101	111	2F	1	1	4	Complement accumulator One's)
NEG	A← $\overline{A}$ + 1	↕	↕	X	↕	X	V	1	↕	11	101	101	ED	2	2	8	complement) Negate acc, (two's
										01	000	100	44				
CCF	CY← $\overline{CY}$	•	•	X	X	X	•	0	↕	00	111	111	3F	1	1	4	Complement) complement carry
SCF	CY← 1	•	•	X	0	X	•	0	1	00	110	111	37	1	1	4	flag
NOP	No operation	•	•	X	•	X	•	•	•	00	000	000	00	1	1	4	Set carry flag
HALT	CPU halted	•	•	X	•	X	•	•	•	01	110	110	76	1	1	4	
DI	IFF - 0	•	•	X	•	X	•	•	•	11	110	011	F3	1	1	4	
EI	IFF - 1	•	•	X	•	X	•	•	•	11	111	011	FB	1	1	4	
IM 0	Set interrupt mode 0	•	•	X	•	X	•	•	•	11	101	101	ED	2	2	8	
										01	000	110	46				
IM 1	Set interrupt mode 1	•	•	X	•	X	•	•	•	11	101	101	ED	2	2	8	
										01	010	110	56				
IM 2	Set interrupt mode 2	•	•	X	•	X	•	•	•	11	101	101	ED	2	2	8	
										01	011	110	5E				

Note: IFF indicates th interrupt enable flip-flop
CY indicates the carry flip-flop
rr is any of the register pairs BC, DE, IY, SP.

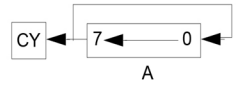
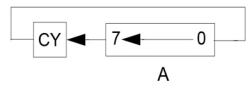
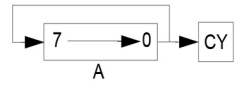
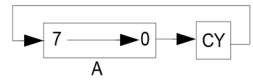
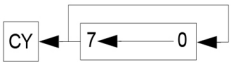
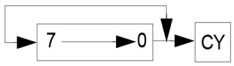
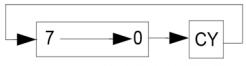
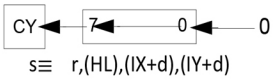
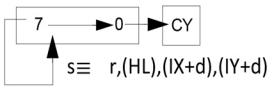
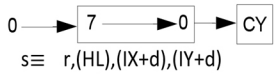
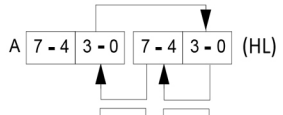
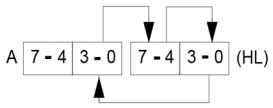
Flog Notation • = flag not affected, 0 = flag reset, 1 = flag set, X = flag is unknown.
↕ = flag is affected according to the result of the operation.

Interrupts are not sampled at the of EI or DI

Mnemonic	Symbolic Operation	Flags								Op-Code				No. of Bytes	No. of M Cycles	No. of T States	Comments
		S	Z		H		P/V	N	C	76	543	210	Hex				
ADD HL,ss	HL ←HL + ss	•	•	X	X	X	•	0	↕	00	ss1	011		1	3	11	ss Reg. 00 BC
ADC HL,ss	HL←HL+ss+CY	↕	↕	X	X	X	V	0	↕	11	101	101	ED	2	4	15	01 DE 10 HL
										01	ss1	010					11 SP
SBC HL, ss	HL←HL-ss-CY	↕	↕	X	X	X	V	1	↕	11	101	101	ED	2	4	15	
										01	ss0	010					
ADD IX, pp	IX ←IX+pp	•	•	X	X	X	•	0	↕	11	011	101	DD	2	4	15	pp Reg. 00 BC
										00	pp1	001					01 DE 10 IX 11 SP
ADD IY, rr	IY ←IY+rr	•	•	X	X	X	•	0	↕	11	111	101	FD	2	4	15	rr Reg. 00 BC
										00	rr1	001					01 DE 10 IY 11 SP
INC ss	ss ← ss + 1	•	•	X	•	X	•	•	•	00	ss0	011		1	1	6	
INC IX	IX ←IX + 1	•	•	X	•	X	•	•	•	11	011	101	DD	2	2	10	
										00	100	011	23				
INC IY	IY ←IY + 1	•	•	X	•	X	•	•	•	11	111	101	FD	2	2	10	
										00	100	011	23				
DEC ss	ss ←ss - 1	•	•	X	•	X	•	•	•	00	ss1	011		1	1	6	
DEC IX	IX ←IX - 1	•	•	X	•	X	•	•	•	11	011	101	DD	2	2	10	
										00	101	011	28				
DEC IY	IY ←IY - 1	•	•	X	•	X	•	•	•	11	111	101	FD	2	2	10	
										00	101	011	28				

Note: ss is any of the register pairs BC, DE, HL, SP
pp is any of the register pairs BC, DE, IX, SP
rr is any of the register pairs BC, DE, IY, SP.

Flog Notation • = flag not affected, 0 = flag reset, 1 = flag set, X = flag is unknown.
↕ = flag is affected according to the result of the operation.

Mnemonic	Symbolic Operation	Flags S	Z		H		P/V	N	C	Op-Code 76	543	210	Hex	No. of Bytes	No. of M Cycles	No. of T States	Comments
RLCA		•	•	X	0	X	•	0	↕	00	000	111	7	1	1	4	Rotate left circular accumulator
RLA		•	•	X	0	X	•	0	↕	00	010	111	17	1	1	4	Rotate left accumulator
RRCA		•	•	X	0	X	•	0	↕	00	001	111	0F	1	1	4	Rotate right circular accumulator
RRA		•	•	X	0	X	•	0	↕	00	011	111	1F	1	1	4	Rotate right accumulater
RLC r		↕	↕	X	0	X	P	0	↕	11 00	001 000	011 r	CB	2	2	8	Rotate left circular accumulater
RLC (HL)		↕	↕	X	0	X	P	0	↕	11	001 000	011 110	CB	2	4	15	r Reg. 000 B 001 C 010 D 011 E 100 H 101 L 111 A
RLC (IX+d)	 r,(HL),(IX+d),(IY+d)	↕	↕	X	0	X	P	0	↕	11 11 ← 00	011 001 d 000	101 011 → 110	DD CB	4	6	23	
RLC (IY+d)		↕	↕	X	0	X	P	0	↕	11 11 ← 00	111 001 d 000	101 011 → 110	FD CB	4	6	23	
RL s	 s≡ r,(HL),(IX+d),(IY+d)	↕	↕	X	0	X	P	0	↕		010						Instruction format and states are as shown for RLC's To form new Op-Code replace 000 Of RLC's With Shown Code
RRC s	 s≡ r,(HL),(IX+d),(IY+d)	↕	↕	X	0	X	P	0	↕		001						
RR s	 s≡ r,(HL),(IX+d),(IY+d)	↕	↕	X	0	X	P	0	↕		011						
SLA s	 s≡ r,(HL),(IX+d),(IY+d)	↕	↕	X	0	X	P	0	↕		100						
SRA s	 s≡ r,(HL),(IX+d),(IY+d)	↕	↕	X	0	X	P	0	↕		101						
SRL s	 s≡ r,(HL),(IX+d),(IY+d)	↕	↕	X	0	X	P	0	↕		111						
RLD		↕	↕	X	0	X	P	0	•	11 01	101 101	101 111	ED 6F	2	5	18	Rotate digit left and right between the accumulator and location (HL). The content of the upper half of the accumulator is unaffcted
RRD		↕	↕	X	0	X	P	0	•	11 01	101 100	101 11	ED 67	2	5	18	

Flog Notation • = flag not affected, 0 = flag reset, 1 = flag set, X = flag is unknown.
↕ = flag is affected according to the result of the operation.

8 – BIT SET, RESET AND TEST GROUP

Mnemonic	Symbolic Operation	Flags								Op-Code				No. of Bytes	No. of M Cycles	No. of T States	Comments
		S	Z		H		P/V	N	C	76	543	210	Hex				
BIT b, r	$Z \leftarrow \overline{r_b}$	X	↕	X	1	X	X	0	•	11	001	011	CB	2	2	8	
										01	b	r					
BIT b, (HL)	$Z \leftarrow \overline{(HL)_b}$	X	↕	X	1	X	X	0	•	11	001	011	CB	2	3	12	
										01	b	110					
BIT b, (IX+d) $_b$	$Z \leftarrow \overline{(IX+d)_b}$	X	↕	X	1	X	X	0	•	11	001	101	DD	4	5	20	
										11	001	011	CB				
										←	d	→					
										01	b	110					
BIT b, (IY+d) $_b$	$Z \leftarrow \overline{(IY+d)_b}$	X	↕	X	1	X	X	0	•	11	111	101	FD	4	5	20	
										11	001	011	CB				
										←	d	→					
										01	b	110					
SET b, r	$r_b \leftarrow 1$	•	•	X	•	X	•	•	•	11	001	011	CB	2	2	8	
										11	b	r					
SET b, (HL)	$(HL)_b \leftarrow 1$	•	•	X	•	X	•	•	•	11	001	011	CB	2	4	15	
										11	b	110					
SET b, (IX+d)	$(IX+d)_b \leftarrow 1$	•	•	X	•	X	•	•	•	11	011	101	DD	4	6	23	
										11	001	11	CB				
										←	d	→					
										11	b	110					
SET b, (IY+d)	$(IY+d)_b \leftarrow 1$	•	•	X	•	X	•	•	•	11	111	101	FD	4	6	23	
										11	001	011	CB				
										←	d	→					
										11	b	110					
RES b, s	$s_b \leftarrow 0$ s ≡ r, (HL), (IX+d), (IY+d)	•	•	X	•	X	•	•	•	10							To from new 0p Code replace 11 of SET b, s with 10 flags and time states states for SET instruction

b	Bit Tested
000	0
001	1
010	2
011	3
100	4
101	5
110	6
111	7

r	Reg.
000	
001	
010	
011	
100	H
101	L
111	A

Note: The notation s_b indictaes bit b (0 to 7) or location s.

Flog Notation • = flag not affected, 0 = flag reset, 1 = flag set, X = flag is unknown.
↕ = flag is affected according to the result of the operation.

Mnemonic	Symbolic Operation	Flags								Op-Code				No. of Bytes	No. of M Cycles	No. of T States	Comments
		S	Z		H		P/V	N	C	76	543	210	Hex				
JP nn	PC ←nn	•	•	X	•	X	•	•	•	11	000	011	C3	3	3	10	
										←	n	→					
										←	n	→					cc Condition
JP cc, nn	if condition cc	•	•	X	•	X	•	•	•	11	cc	010		3	3	10	000 Z non zero
	is true PC ←nn,									←	n	→					001 zero
	other wise									←	n	→					010 C non carry
	continue																011 arry
																	100 O parity odd
																	101 E parity even
																	110 sing positive
JR e	PC ← PC + e	•	•	X	•	X	•	•	•	00	011	000	18	2	3	12	111 ing negative
										←	e - 2	→					
JR C, e	if C = 0,	•	•	X	•	X	•	•	•	00	111	000	38	2	2	7	if condition not met
	continue									←	e - 2	→					
	if C = 1,													2	3	12	if condition is met
	PC ← PC + e																
JR NC, e	if C = 1,	•	•	X	•	X	•	•	•	00	110	000	30	2	2	7	if condition not met
	continue									←	e - 2	→					
	if C = 0,													2	3	12	if condition is met
	PC ← PC + e																
JR Z, e	if Z = 0	•	•	X	•	X	•	•	•	00	101	000	28	2	2	7	if condition not met
	continue									←	e - 2	→					
	if Z = 1,													2	3	12	if condition is met
	PC ← PC + e																
JR NZ, e	if Z = 1,	•	•	X	•	X	•	•	•	00	100	000	20	2	2	7	if condition not met
	continue									←	e - 2	→					
	if Z = 0,													2	3	12	if condition is met
	PC ← PC + e																
JP (HL)	PC ← HL	•	•	X	•	X	•	•	•	11	101	001	E9	1	1	4	
JP (IX)	PC ← IX	•	•	X	•	X	•	•	•	11	011	101	DD	2	2	8	
										11	101	001	E9				
JP (IY)	PC ← IY	•	•	X	•	X	•	•	•	11	111	101	FD	2	2	8	
										11	101	001	E9				
DJNZ, e	B ← B - 1	•	•	X	•	X	•	•	•	00	010	000	10	2	2	8	if B = 0
	if B = 0									←	e - 2	→					
	continue																
	if B ≠ 0													2	2	13	if B ≠ 0
	PC ← PC + e																

Note: e represnts the extension in the realtive addressing mode.
e is a signd two's complement numbr in the range <126, 129>
e - 2 in the op-code provides an effective address of PC + e as PC is incremented by 2 prior to the addition of e.

Flag Notation: • = flag not affected, 0 = flag is reset, 1 = flag is set, X = flag is unknown

↕ = flag is affcted according to the result of the operation

CALL AND RETURN GROUP

Mnemonic	Symbolic Operation	Flags S	Z		H		P/V	N	C	Op-Code 76	543	210	Hex	No. of Bytes	No. of M Cycles	No. of T States	Comments
CALL nn	(SP.1) ←PC $_H$ (SP.2) ←PC $_L$ PC ← nn	•	•	X	•	X	•	•	•	11 ← ←	001 n n	101 → →	CD	3	5	17	
CALL cc, nn	if condition cc is false	•	•	X	•	X	•	•	•	11 ←	cc n	100 →		3	3	10	if cc is false
	continue otherwise same as CALL nn									←	n	→		3	5	17	if cc is true
RET	PC $_L$ ←(SP) PC ←(SP+1)	•	•	X	•	X	•	•	•	11	001	001	C9	1	3	10	
RET $_{CC}$	if condition cc is false	•	•	X	•	X	•	•	•	11	cc	000		1	1	5	if cc is false
	continue otherwise same as RET													1	3	11	if cc is true
RETI	Return from interrupt	•	•	X	•	X	•	•	•	11 01	101 001	101 101	ED 4D	2	4	14	
RETN [1]	Return from non maskable interrupt	•	•	X	•	X	•	•	•	11 01	101 000	101 101	ED 45	2	4	14	
RST $_p$	(SP-1) ←PC $_H$ (SP-2) ←PC $_L$ PC $_H$ ← 0 PC $_L$ ← p	•	•	X	•	X	•	•	•	11	t	111		1	3	11	

cc	Condition
000	Z non zero
001	Z zero
010	NC non carry
011	C carry
100	PO parity odd
101	PE parity even
110	P sing positive
111	M sing negative

t	p
000	0H
001	8H
010	0H
011	8H
100	0H
101	8H
110	0H
111	8H

Note: [1] Instruction also IFF $_2$← IFF $_1$

Flag Notation: • = flag not affected, 0 = flag is reset, 1 = flag is set, X = flag is unknown
↕ = flag is affcted according to the result of the operation

Mnemonic	Symbolic Operation	Flags								Op-Code				No. of Bytes	No. of M Cycles	No. of T States	Comments
		S	Z		H		P/V	N	C	76	543	210	Hex				
IN A, (n)	A ← (n)	•	•	X	•	X	•	•	•	11	011	011	DB	2	3	11	n to $A_0 \sim A_7$ Acc to $A_8 \sim A_{15}$
										←	n	→					
IN r, (C)	r ← (C) if r = 110 only the flags will be affected	↕	↕	X	↕	X	P	0	•	11 01	101 r	101 000	ED	2	3	12	C to $A_0 \sim A_7$ B to $A_8 \sim A_{15}$
INI	(HL) ← (C) B ← B - 1 HL ← HL + 1	X	① ↕	X	X	X	X	1	X	11 10	101 100	101 010	ED A2	2	4	16	C to $A_0 \sim A_7$ B to $A_8 \sim A_{15}$
INIR	(HL) ← (C) B ← B - 1 HL ← HL + 1 Repat until B = 0	X	1	X	X	X	X	1	X	11 10	101 110	101 010	ED B2	2 2	5 (if B ≠ 0) 4 (if B = 0)	21 16	C to $A_0 \sim A_7$ B to $A_8 \sim A_{15}$
IND	(HL) ← (C) B ← B - 1 HL ← HL - 1	X	① ↕	X	X	X	X	1	X	11 10	101 101	101 010	ED AA	2	4	16	C to $A_0 \sim A_7$ B to $A_8 \sim A_{15}$
INDR	(HL) ← (C) B ← B - 1 HL ← HL - 1 Repat until B = 0	X	↕	X	X	X	X	1	X	11 10	101 111	101 010	ED BA	2 2	5 (if B ≠ 0) 4 (if B = 0)	21 16	C to $A_0 \sim A_7$ B to $A_8 \sim A_{15}$
OUT (n), A	(n) ← A	•	•	X	•	X	•	•	•	11	010	011	D3	2	3	11	n to $A_0 \sim A_7$ Acc to $A_8 \sim A_{15}$
OUT (C), r	(C) ← r	•	•	X	•	X	•	•	•	11 01	101 r	101 001	ED	2	3	12	C to $A_0 \sim A_7$ B to A_8 A_{15}
OUTI	(C) ← (HL) B ← B - 1 HL ← HL + 1	X	① ↕	X	X	X	X	1	X	11 10	101 100	101 011	ED A3	2	4	16	C to $A_0 \sim A_7$ B to $A_8 \sim A_{15}$
OTIR	(C) ← (HL) B ← B - 1 HL ← HL + 1 Repat until B = 0	X	↕	X	X	X	X	1	X	11 10	101 100	101 011	ED B3	2 2	5 (if B ≠ 0) 4 (if B = 0)	21 16	C to $A_0 \sim A_7$ B to $A_8 \sim A_{15}$
OUTD	(C) ← (HL) B ← B - 1 HL ← HL - 1	X	① ↕	X	X	X	X	1	X	11 10	101 101	101 011	ED AB	2	4	16	C to $A_0 \sim A_7$ B to $A_8 \sim A_{15}$
OTDR	(C) ← (HL) B ← B - 1 HL ← HL - 1 Repat until B = 0	X	① ↕	X	X	X	X	1	X	11 10	101 111	101 011	ED BB	2 2	5 (if B ≠ 0) 4 (if B = 0)	21 16	C to $A_0 \sim A_7$ B to $A_8 \sim A_{15}$

Note: ① f the result of B - 1 is zero the Z flag is set, otherwis it is reset

Flog Notation • = flag not affected, 0 = flag reset, 1 = flag set, X = flag is unknown.
↕ = flag is affected according to the result of the operation.